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Optimization of Area, Power, and Delay in BCD to Seven segment decoder using MGDI Technique

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ABSTRACT-Seven segment displays are the most common device used for displaying digits and alphabets. The Majority of applications such as calculators, washing machines, radios, digital clocks, etc, uses seven-segment displays to give a visual token of numbers and alphabets. The binary value can be displayed in the form of decimal using this seven-segment display. The seven-segment displays are made up of LEDs (Light-emitting diode). Single seven segment or multiple segments are arranged in an order that meets our requirements. The special BCD to 7 segment display decoder integrated circuit is used in converting the incoming BCD signal to a form convenient for activating these displays. IC 74LS47 designed by Fairchild Semiconductor is known for BCD to 7 segment display decoder practically. The drawback of the 74LS47 IC is that it consumes significant power. In this work, a modified BCD to seven-segment display decoder is implemented using the MGDI technique which consumes lesser power compared to the conventional complementary CMOS logic.

Index Terms – CMOS logic, MGDI Technique, Seven Segment decoder

I. INTRODUCTION

Seven segment display consists of 7 LEDs, by forward biasing the appropriate pins of the LED segments in a particular sequence, some segments will be light and others will be blank allowing the desired digit to be generated on the display. This allows us to display each of the ten decimal digits from 0 to 9 on the same 7-segment display.

Seven segment display is differentiated into two types based on the connection, those are,

- **Common cathode LED display:** Logic 1 applied to the segments which have to be in ON condition and Logic 0 applied to the segments which have to be in off condition.
- **Common anode display:** Logic 0 applied to the segments which have to be in ON condition and Logic 1 applied to the segments which have to be in off condition.

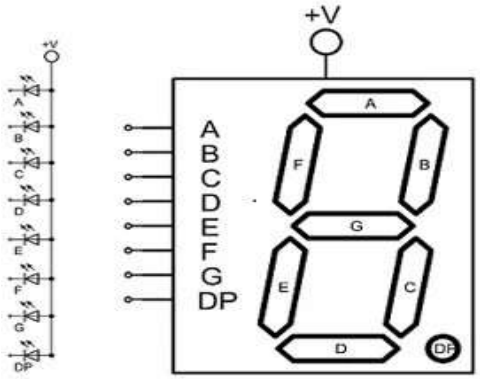

Figure 1 Seven segment common anode display

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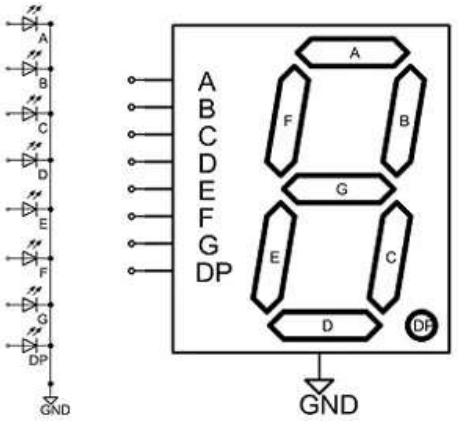

Figure 2 Seven segment common cathode display

A BCD to 7 segment display decoder is a digital combinational logic circuit that receives a decimal integer digit in Binary Coded Decimal format as inputs and produces applicable outputs for the segments to exhibit the applied input decimal digit. The operation of the BCD to 7 segment display decoder is illustrated in the form of a truth table and is exhibited in Table 1

Table 1 Decoder truth table

Decimal Digit	Input lines				Output lines						
	A	B	C	D	a	b	c	d	e	f	g
0	0	0	0	0	1	1	1	1	1	1	0
1	0	0	0	1	0	1	1	0	0	0	0
2	0	0	1	0	1	1	0	1	1	0	1
3	0	0	1	1	1	1	1	1	0	0	1
4	0	1	0	0	0	1	1	0	0	1	1
5	0	1	0	1	1	0	1	1	0	1	1
6	0	1	1	0	1	0	1	1	1	1	1
7	0	1	1	1	1	1	1	0	0	0	0
8	1	0	0	0	1	1	1	1	1	1	1
9	1	0	0	1	1	1	1	1	0	1	1

The expression for output lines is realized using the k-map technique. And those expressions are given below
a = A + C + BD + B'D'
b = B' + C'D' + CD
c = C' + D + B
d = A + B'D' + CD' + B'C + BC'D
e = B'D' + CD'
f = A + C'D' + BD' + BC'
g = A + BC' + CD' + B'C

The logic diagram for BCD to seven-segment display decoder is depicted in Fig. 3.

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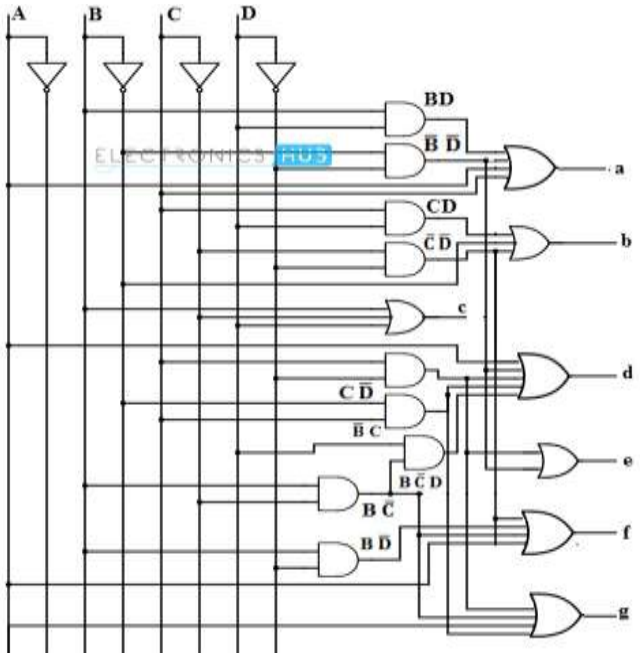

Figure 3 Gate level design of BCD to 7 Segment Display

II. LITERATURE SURVEY

ASIC design blocks of the digital logic system and some of the fundamental combinational circuits are designed and simulated using GDI and other conventional complementary CMOS design techniques. Parallel adders such as Ripple carry adder, Look ahead adder, and magnitude comparator circuits were designed and implemented in GDI and other parallel design methodologies. From the reference [1] it is revealed that circuit implementation using the GDI technique consumes more power than the MGDI technique.

The performance analysis of MGDI, GDI, and CMOS logic is presented in reference [2]. The performance analysis is made for switching transistor count, delay, and total average power consumed by MGDI, GDI, and CMOS logic. From this analysis, it is observed that the modified Gate Diffusion Input performance is better when comparing to CMOS and GDI logic. In CMOS the number of transistors used to realize a function is double that of MGDI. The transistors used to design XOR and XNOR has only 3 transistors in MGDI whereas it is 8 in CMOS logic. The power consumed by CMOS logic is slightly higher than that of MGDI.

The DM74LS47 accepts 4 lines of BCD input data, generates their complements internally, and decodes the info with seven AND/OR gates having open-collector outputs to drive indicator segments directly. Each segment output is sure to sink 24 mA in the ON state (LOW) and withstand 15V in the OFF state (HIGH) with a maximum leakage current of 250µA. Auxiliary inputs provided blanking, lamp test, and cascadable zero-suppression functions. These general and functionality descriptions are referred from reference [3].

III. METHODOLOGY

The basic primitive of the GDI cell consists of nMOS and pMOS containing four terminals G (common gate input of nMOS and pMOS transistors), P (the outer diffusion node of the pMOS transistor), N (the outer diffusion node of the nMOS transistor), and D (common diffusion node of both transistors). The structure of basic GDI is shown in Fig. 4

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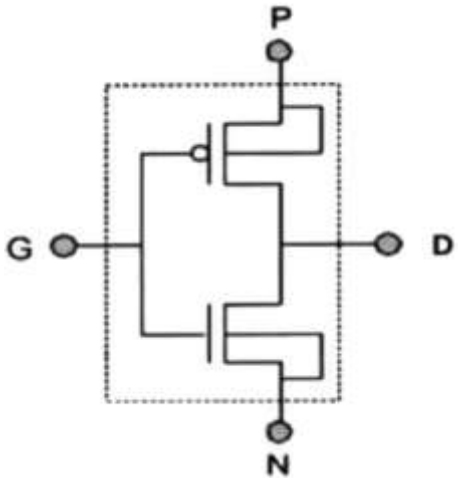

Figure 4 Basic GDI Cell

Different input configuration which is applied to GDI cell can make it to perform various Boolean functions. Although the GDI technique poses the above-mentioned advantages such as fast, low power dissipation, and occupies a small cell area, the full swing output cannot be achieved in the circuits designed using the MGDI technique. The input configurations for different MGDI gates are shown below.

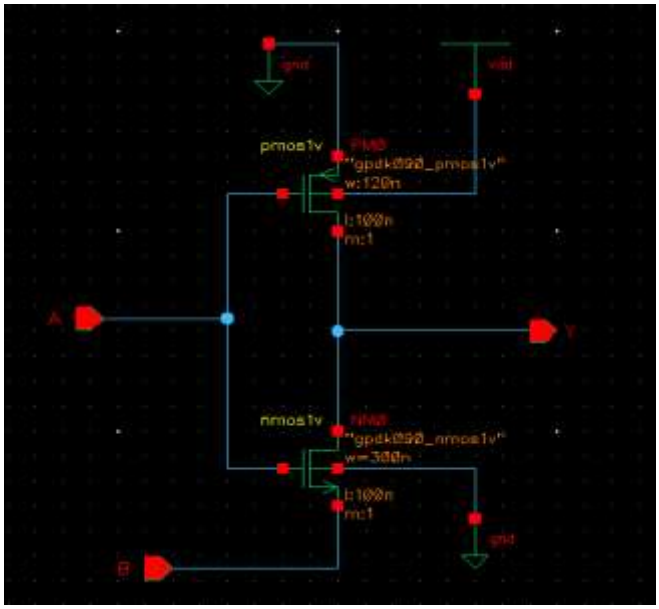

Figure 5 MGDI AND Gate

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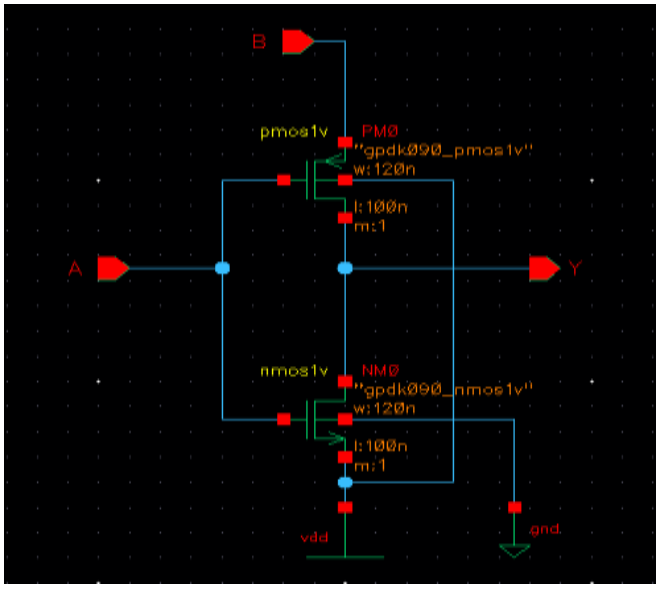

Figure 6 MGDI OR Gate

In this work, a modified primitive GDI logic gates have been implemented in 90gpdk technology and it is compared with existing CMOS logic. The designed decoder is shown in Fig 7.

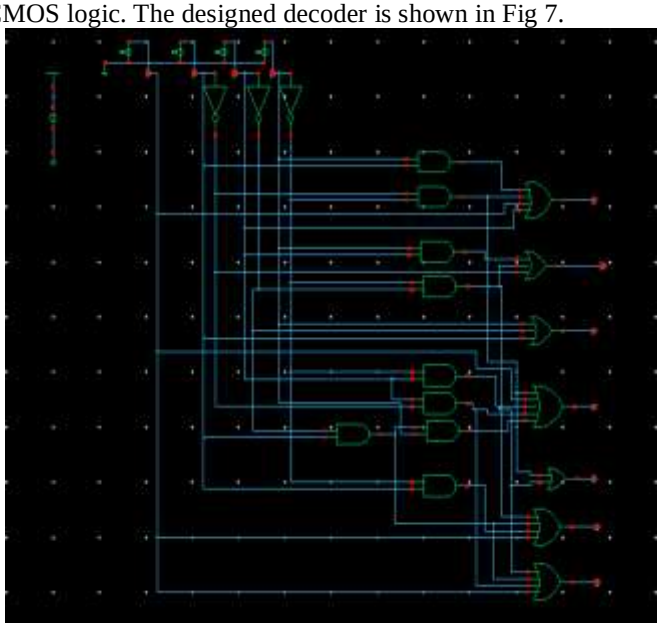

Figure 7 Designed decoder circuit

In this work, BCD to 7 Segment display decoder has been constructed and implemented using Modified Gate Diffusion Input technique. Implementation has been performed using Cadence virtuoso. Comparison is made with the parameters power, delay, and area. The area is provided by the usage of the number of gates. It is found that MGDI based BCD to seven segment display decoder achieves better performance corresponding to the area, power and delay. Table 2 shows the comparative analysis of the above-mentioned techniques.

Table 2 Result Comparison table

Technique	No of gates	Power	Delay
CMOS Based Design	162	68mW	100nS
MGDI Based Design	76	10.076mW	0.801nS

IV. CONCLUSION

In this work, the design implementation of BCD to seven segment display decoder has been made using the MGDI technique. The suggested MGDI design is simulated using Cadence 90nm technology. The simulation results show that the MGDI based BCD to seven-segment display decoder consumes 85.19% less power, 53% less area and operates with 99.19% high speed compared to the existing Complementary CMOS gates based BCD to seven segment display decoder.

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